IN THE CLAIMS

1-42. (Canceled)

43. (New) A clock generating method comprising the steps of:

providing a plurality of circuit blocks, a plurality of separate oscillators each having an oscillation node, and a conductive wiring line, oscillation nodes of the plurality of separate oscillators being connected to the conductive wiring line at spaced intervals of length along the conductive wiring line;

synchronizing oscillation signals outputted from each of the plurality of separate oscillators; and

supplying the oscillating signals to each of the plurality of circuit blocks from each of the plurality of separate oscillators respectively.

44. (New) A clock generating method, according to claim 43,

wherein each of the plurality of separate oscillators is a ring oscillator including a plurality of inverters; and

wherein an output of one of the plurality of inverters is connected to both the conductive wiring line and an input of another of the plurality of inverters.

45. (New) A clock generating method, according to claim 43,

wherein a shape of the conductive wiring line is a closed loop.

46. (New) A clock generating method, according to claim 43,

wherein a shape of the conductive wiring line is a mesh; and

wherein the oscillation nodes are connected at intersection points of the mesh respectively.

47. (New) A clock generating method, according to claim 43,

wherein the spaced intervals of length are substantially equal.

48. (New) A clock generating method, according to claim 44,

wherein the spaced intervals of length and load driving capabilities of the plurality of inverters are determined so that the plurality of separate oscillators are synchronized to oscillate with a substantially identically frequency at each of the oscillation nodes.

49. (New) A clock generating method, according to claim 48,

wherein the spaced intervals of length and load driving capabilities of the inverters are determined so that the plurality of separate oscillators are synchronized to oscillate with a substantially identically phase at each of the oscillation nodes.

50. (New) A clock generating method comprising the steps of:

providing a plurality of circuit blocks each having a clock distribution network, a frequency divider dividing a clock signal of the clock distribution network of one of the circuit blocks, a phase/frequency comparator comparing the clock signal divided by the frequency divider with a reference clock signal and outputting an error signal, a plurality of separate voltage-controlled oscillators each having an

oscillation node and outputting an oscillation signal in accordance with the error signal, and a conductive wiring line, oscillation nodes of the plurality of separate voltage-controlled oscillators being connected to the conductive wiring line at spaced intervals of length along the conductive wiring line;

synchronizing oscillation signals outputted from each of the plurality of separate oscillators; and

supplying the oscillating signals to each of the plurality of circuit blocks from each of the plurality of separate oscillators respectively.

51. (New) A clock generating method, according to claim 50,

wherein each of the plurality of voltage-controlled oscillators includes a plurality of inverters whose delay is variable in accordance with the error signal; and

wherein an output of one of the plurality of inverters is connected to both the conductive wiring line and an input of another of the plurality of inverters.

52. (New) A clock generating method, according to claim 50,

wherein a shape of the conductive wiring line is a closed loop.

53. (New) A clock generating method, according to claim 50,

wherein a shape of the conductive wiring line is a mesh;

wherein the oscillation nodes are connected at intersection points of the mesh respectively.

54. (New) A clock generating method, according to claim 50,

wherein the intervals of length are substantially equal.

55. (New) A clock generating method, according to claim 51,

wherein the spaced intervals of length and load driving capabilities of the inverters are determined so that the oscillators are synchronized to oscillate with a substantially identically frequency at each of the oscillation nodes.

56. (New) A clock generating method, according to claim 55,

wherein the spaced intervals of length and load driving capabilities of the inverters are determined so that the oscillators are synchronized to oscillate with a substantially identically phase at each of the oscillation nodes.

57. (New) A clock generating method comprising the steps of:

providing a plurality of circuit blocks, a plurality of separate oscillators each having an oscillation node, and a conductive wiring line, oscillation nodes of the plurality of separate oscillators being connected to the conductive wiring line at spaced intervals of length along the conductive wiring line;

synchronizing oscillation signals outputted from each of the plurality of separate oscillators; and

supplying the oscillating signals to each of the plurality of circuit blocks from each of the plurality of separate oscillators respectively, such that a clock feed range of each oscillator is reduced, thereby reducing overall clock skew for the semiconductor integrated circuit device.

58. (New) A clock generating method, according to claim 43, wherein the conductive wiring line is provided with a plurality of switches such that only certain ones of the plurality of separate oscillators are operated at any one time in order to selectively lower power dissipation.

59. (New) A clock generating method, according to claim 50, wherein the conductive wiring line is provided with a plurality of switches such that only certain ones of the plurality of separate voltage-controlled oscillators are operated at any one time in order to selectively lower power dissipation.

60. (New) A clock generating method, according to claim 43, wherein the oscillation nodes can both receive an input signal from the conductive wiring line and output an oscillation signal to the conductive wiring line.

61. (New) A clock generating method, according to claim 50, wherein the oscillation nodes can both receive an input signal from the conductive wiring line and output an oscillation signal to the conductive wiring line.

62. (New) A clock generating method, according to claim 57, wherein the oscillation nodes can both receive an input signal from the conductive wiring line and output an oscillation signal to the conductive wiring line.